What is claimed is:

1. A logical operation circuit comprising:

a ferroelectric capacitor which can retain a polarization state corresponding to first operation target data and which has first and second terminals;

a first signal line connected to the first terminal;

a second signal line which can provide second operation target data to the second terminal of the ferroelectric capacitor retaining the polarization state corresponding to the first operation target data and which is connected to the second terminal; and

an operation result output section which outputs the result of a logical operation on the first and second operation target data based on a polarization state of the ferroelectric capacitor generated by providing the second operation target data to the ferroelectric capacitor and which is connected to the first signal line.

2. The logical operation circuit as set forth in Claim 1, wherein the first and second signal lines are connected to one of first and second reference potentials and the other of the first and second reference potentials, respectively, to generate the polarization state corresponding to the first operation target data in the ferroelectric capacitor.

3. The logical operation circuit as set forth in Claim 1

or 2,

wherein the operation result output section has an electric field effect transistor as an output transistor which has a gate terminal connected to the first signal line and an output terminal for outputting an output signal corresponding to a control signal inputted into the gate terminal, and which becomes off when a potential on the first reference potential side from its threshold voltage is given as the control signal and becomes on when a potential on the second reference potential side from its threshold voltage is given as the control signal, and

wherein the result of the logical operation is obtained as an output signal from the output transistor.

4. The logical operation circuit as set forth in Claim 3,

wherein the first signal line can be connected to the second reference potential to precharge the first terminal of the ferroelectric capacitor retaining the polarization state corresponding to the first operation target data to the second reference potential, and

wherein, when the result of the logical operation is outputted, the first signal line is connected to the second reference potential and the connection is released, then the second signal line is connected to the first or second reference potential corresponding to the second operation target data, and the result of the logical operation is outputted based on a potential which is generated in the first signal line when

the second signal line is connected to the first or second reference potential corresponding to the second operation target data.

5. A logical operation circuit comprising:

a ferroelectric capacitor having first and second terminals;

first and second signal lines connected to the first and second terminals, respectively; and

an electric field effect transistor as an output transistor which has a gate terminal connected to the first signal line and an output terminal for outputting an output signal corresponding to a control signal inputted into the gate terminal, and which becomes off when a potential on a first reference potential side from its threshold voltage is given as the control signal and becomes on when a potential on a second reference potential side from its threshold voltage is given as the control signal,

wherein the first and second signal lines are connected to one of the first and second reference potentials and the other of the first and second potentials, respectively, to generate a polarization state corresponding to first operation target data in the ferroelectric capacitor,

the first and second signal lines are then both connected to the second reference potential to precharge the first signal line to the second reference potential without causing a change in the residual polarization state of the ferroelectric

capacitor, and

the application of voltage to the first signal line is stopped and the second signal line is connected to the first or second reference potential corresponding to second operation target data, and an output signal produced at the output terminal of the output transistor in response to a potential which is generated in the first signal line when the second signal line is connected to the first or second reference potential corresponding to the second operation target data is obtained as the result of a logical operation on the first and second operation target data.

6. The logical operation circuit as set forth in Claim 4 or 5,

wherein the absolute value Vath of the difference between the threshold voltage of the output transistor and the first reference potential is equal to or higher than the coercive electric field Vc of the ferroelectric capacitor and satisfies the following relation:

$CG \leq Pr/(Vd - Vc)$ and $CFnon/CG + 1 < Vd/Vath$

wherein

CG: the gate capacitance of the output transistor,

CFnon: the average capacitance of the ferroelectric capacitor in the non-inversion direction,

Pr: the residual polarization of the ferroelectric capacitor, and

Vd: the absolute value of the difference between the first and

second reference potentials.

7. The logical operation circuit as set forth in Claim 4 or 5,

wherein the absolute value Vath of the difference between the threshold voltage of the output transistor and the first reference potential is smaller than the coercive electric field Vc of the ferroelectric capacitor and satisfies the following relation:

$$CFnon/CG + 1 < Vd/Vath < CFrev/CG + 1$$

wherein

CG: the gate capacitance of the output transistor,

CFnon: the average capacitance of the ferroelectric capacitor in the non-inversion direction,

CFrev: the average capacitance of the ferroelectric capacitor in the inversion direction, and

Vd: the absolute value of the difference between the first and second reference potentials.

8. A logical operation circuit comprising:

a non-volatile memory element which can retain a non-volatile state corresponding to first operation target binary data y and which has first and second terminals; and

an operation result output section which outputs, based on a state of the non-volatile memory element generated by providing second operation target binary data x to the second terminal of the non-volatile memory element, the result of a

logical operation on the first and second operation target binary data x and y as operation result binary data z,

wherein the operation result binary data z substantially satisfies the following relation:

z = x AND y.

9. The logical operation circuit as set forth in Claim 8,

wherein the non-volatile memory element includes a ferroelectric capacitor and the non-volatile state is a residual polarization state of the ferroelectric capacitor.

10. A logical operation circuit comprising:

a non-volatile memory element which can retain a non-volatile state corresponding to first operation target data; and

an operation result output section which outputs, based on a state of the non-volatile memory element generated by providing second operation target data to the non-volatile memory element, the result of a logical operation on the first and second operation target data and which is connected to a first terminal of the non-volatile memory element.

11. A logical operation device comprising a plurality of logical operation circuits according to any one of Claims 1 to 10 which are arranges in series and/or parallel to perform a desired operation.

12. A logical operation device comprising:

a retrieval word retaining section for retaining a retrieval word as a retrieving target; and

a word circuit for retaining a reference word as a referencing target and determining the coincidence between the reference word and the retrieval word,

the word circuit comprising a plurality of logical operation circuits according to any one of Claims 1 to 10 which are arranges in series and/or parallel.

13. The logical operation device as set forth in Claim 12,

wherein the word circuit calculates logical values corresponding to EXNORs of bit values of the reference word and corresponding bit values of the retrieval word using pairs of logical operation circuits connected in series for each of bits constituting the reference word, calculates a logical value corresponding to the AND of all the logical values corresponding to the EXNORs calculated for each of the bits by connecting all the outputs from the pairs of logical operation circuits in parallel, and provides the logical value corresponding to the AND as its coincidence determining output.

14. A logical operation method comprising the steps of:

causing a first ferroelectric capacitor having first and second terminals to retain a polarization state corresponding to first operation target data;

charging the first terminal of the ferroelectric capacitor

retaining the polarization state to a specified reference potential; and

obtaining, based on a polarization state of the ferroelectric capacitor generated by providing second operation target data to the second terminal of the ferroelectric capacitor with the first terminal of the ferroelectric capacitor charged to the specified reference potential, the result of a logical operation on the first and second operation target data.